12. (Amended) The method of claim 11 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. (Amended) The method of claim 11 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.

REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 1-8 and 11-15 are pending in this application. Claims 1-8 and 12-15 are rejected. The indication by the Examiner that claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims, is further noted and appreciated.

Claim 11 has been amended to include all of the limitations in the base claim 1. A reconsideration for allowance of claim 11 is respectfully requested of the Examiner.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 3-7 and 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al. '117 in view of Haq '677.

67,200-327
Serial Number 09/885,784

Independent claim 1 has been cancelled and withdrawn from further consideration by the Examiner. The dependency of claims 2-6 and 12-13 have been changed to the newly amended independent claim 11, which the Examiner has indicated would be allowable if rewritten into independent form to include all of the limitations of the base claim 1. Dependent claim 7 depends on claim 6, which in turn depends on independent claim 11.

A reconsideration for allowance of claims 3-7 and 12-13 is therefore respectfully requested of the Examiner.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al in view of Haq and further in view of Davidson '010.

Claim 2 has been amended to change its dependency from claim 1 to claim 11, which is now believed to be allowable. A reconsideration for allowance of claim 2 is respectfully requested of the Examiner.

Claims 8, 14 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al in view of Kresge et al '808.

Claims 14 and 15 have been cancelled and withdrawn from further consideration by the Examiner.

67,200-327
Serial Number 09/885,784

Claim 8 has been amended to change its dependency from claim 1 to claim 11, which is now believed to be allowable. A reconsideration for allowance of claim 8 is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 2-8 and 11-13, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made". In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040

RWT\kd

67,200-327
Serial Number 09/885,784

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please cancel claims 1 and 14-15.

Please amend claims 2-6, 8 and 11-13 as follows.

2. (Amended) The method of claim [1] 11 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. (Amended) The method of claim [1] 11 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. (Amended) The method of claim [1] 11 wherein the second substrate is a second semiconductor substrate.

5. (Amended) The method of claim [1] 11 wherein the first semiconductor substrate is thicker than the second substrate.

6. (Amended) The method of claim [1] 11 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

8. (Amended) The method of claim [1] 11 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

11. (Amended) [The] A [of claim 1 wherein the] method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication;

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a

laminated completely fabricated semiconductor integrated circuit microelectronic fabrication; and

removing the second substrate from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, said planarizing methods employ said dielectric isolated metallization pattern as a stop layer.

12. (Amended) The method of claim [1] 11 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. (Amended) The method of claim [1] 11 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.